B.Tech IV Year I Semester

JNTUA COLLEGE OF ENGINEERING (AUTONOMOUS) PULIVENDULA

19AEC75c-BASICS OF VLSI DESIGN

(Open Elective-III)

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Course Objectives: The objectives of the course are to make the students learn about

- To give exposure to different steps involved in the fabrication of ICs and electrical properties of MOS devices.
- To know the design rules in drawing the layout of any logic circuit.
- To design different types of logic gates using CMOS inverter and analyze their transfer characteristics.
- To learn the concepts scaling and designing building blocks of data path of any system using gates.
- Understand the design and operation of basic programmable logic devices.

UNIT – I:

MOS Technology: Introduction to IC Technology. The IC Era, MOS and related VLSI Technology, Basic MOS Transistors, Enhancement and Depletion modes of transistor action, nMOS and CMOS Fabrication processes.

Basic Electrical Properties of MOS Circuits: I_{ds} versus V_{ds} Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Transconductance and Output Conductance, nMOS Inverter, Determination of Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, CMOS Inverter.

Learning Outcomes:

At the end of this unit, the student will be able to

- Understand different steps involved in the fabrication of ICs and electrical properties of MOS devices. **L2**
- Analyze the operation of NMOS, CMOS and BiCMOS inverters. **L4**

UNIT – II:

MOS Circuit Design Processes: MOS Layers, Stick Diagrams, Design Rules and Layout, General observations on the Design rules, 2μm Double Metal, Double Poly CMOS rules, Layout Diagrams-A Brief Introduction, Symbolic Diagrams-Translation to Mask Form.

Learning Outcomes:

At the end of this unit, the student will be able to

- Know the VLSI design flow and stick diagrams. **L1**
- Understand the design rules in drawing the layout of any logic circuit. **L2**

UNIT – III:

Basic Circuit Concepts: Sheet Resistance. Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, standard unit of capacitance, area Capacitance calculations, the Delay Unit, Inverter Delays, Driving large capacitive loads, Propagation Delays, Wiring Capacitances.

Learning Outcomes:

At the end of this unit, the student will be able to

- Understand different types of logics in gate level design. **L2**
- Learn and compare different performance parameters in gate level design. **L1**

UNIT – IV:

Scaling of MOS Circuits: Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling.

Sub System Design and Layout: Switch logic, Gate logic, Examples of Structured Design, parity generator, multiplexers, and grey to binary code converter.

Learning Outcomes:

At the end of this unit, the student will be able to

- Appreciate the importance, models and limitations of scaling. **L1**
- Explain the building blocks of data path of any system using gates. **L1**

UNIT – V:

Programmable Logic Devices: Read only memories, Programmable Logic Arrays (PLA), Programmable Array Logic (PAL), Complex programmable logic devices, Field programmable gate arrays.

Learning Outcomes:

At the end of this unit, the student will be able to

- Explain different programmable logic devices. **L1**
- Compare the performance parameters and applications of different programmable logic devices. **L2**

Text Books:

1. Kamran Eshraghian. Douglas, A. Pucknell and Sholeh Eshraghian, "Essentials of LSI Circuits and Systems", Prentice Hall of India Private Limited, 2005 Edition.
2. Neil H.E.WESTE, David Harris andAyan Banerjee, "CMOS VLSI Design A Circuits and systems perspective", Pearson Education, 2006 Third Edition

Reference Books:

1. Richa Jain and Amrita Rai, "Principles of VLSI and CMOS Integrated Circuits", S.Chand and Company Limited. First edition.2012.
2. Wayne Wolf, "Modern VLSI Design", Pearson Education, 3rd Edition.

Course Outcomes:

At the end of this Course the student will be able to

- Understand different steps involved in the fabrication of ICs and electrical properties of MOS devices. **L2**
- Know the design rules in drawing the layout of any logic circuit. **L1**
- Compare different types of logic gates using CMOS inverter and their transfer characteristics. **L2**
- Learn the concepts to design building blocks of data path of any system using gates. **L1**
- Gain knowledge about basic programmable logic devices and testing of CMOS circuits. **L1**